Novelty Journals

ISSN 2394-9678

International Journal of Novel Research in Electrical and Mechanical Engineering
Vol. 5, Issue 1, pp: (11-18), Month: September 2017 - August 2018, Available at: www.noveltyjournals.com

Designing Low Power Subthreshold Logic Circuits Using AFE

[1*]M. MAHALAKSHMI, [2]P. THIRUVALAR SELVAN

[1]PG Student, [2]Assistant Professor, VLSI Design, Department of ECE, TRP Engineering College, Trichy
*Corresponding Email Id: maha28.ece@gmail.com

Abstract: **The present scenario the circuit subthreshold CMOS logic circuits are becoming increasingly popular energy- constrained applications where high performance is not required. Minimum energy consumption of digital logic circuits can be obtained by operating in the subthreshold regime. However, in this regime process variations can result in up to order of magnitude variations in I_{ON} / I_{OFF} ratios leading to timing errors, which can have a destructive effect on the functionality of the subthreshold circuits. These timing errors become more frequent in scaled technology nodes where process variations are highly prevalent. Therefore, mechanisms to mitigate these timing errors while minimizing the energy consumption are required. In this proposed work, Low power subthreshold logic circuits using adaptive feedback equalizer circuit is designed. The adaptive equalizer technique is used with a sequential digital logic to mitigate the process variation effects and reduce the dominant leakage energy components in the subthreshold digital logic circuits. The performance of the proper circuit is evaluated for different input voltages. This work can be extended by the scaling down the technology to reduce the minimum power consumption.**

Keywords: **Index Terms, Adaptive Feedback equalizer, Low power subthreshold, variable threshold inverter.**

I. INTRODUCTION

The use of subthreshold digital CMOS logic circuits is becoming increasingly popular in energy-constrained applications where high performance is not required. The main idea here is that scaling down the supply voltage can significantly reduce the dynamic energy consumed by digital circuits. Scaling the supply voltage also lowers down the leakage current due to a reduction in the drain-induced barrier lowering (DIBL) effect. However, as the supply voltage is scaled below the threshold voltage of the transistors, the propagation delay of the logic gates increases, which in turn increases the leakage energy of the transistors. These two opposite trends in the leakage and the dynamic energy components lead to a minimum energy supply voltage that occurs below the threshold voltage of the transistors for digital logic circuits [1]. However, digital logic circuits operating in the subthreshold region suffer from process variations that directly affect the threshold voltage (V_T). This, in turn, has a significant impact on the drive current due to the exponential relationship between the drive current and the threshold voltage of the transistors in the subthreshold regime. Moreover, subthreshold digital circuits suffer from the degraded I_{ON} / I_{OFF} ratios [2] resulting in a failure in providing rail-to-rail output swings when restricted by aggressive timing constraints. These degraded I_{ON} / I_{OFF} ratios and process-related variations make subthreshold circuits highly susceptible to timing errors that can further lead to complete system failures. Since the standard deviation of V_T varies inversely with the square root of the channel area [3], one approach to overcome the process variation is to upsize the transistors [2]. Alternately, one can increase the logic path depth to leverage the statistical averaging of the delay across gates [4] to overcome process variations. These approaches, however, increase the transistor parasitics, which in turn increases the energy consumption. In this paper, we first propose the use of a feedback equalizer circuit for lowering the energy consumption of digital logic operating in the subthreshold region while achieving robustness equivalent to that provided by [2]. Here, the feedback equalizer circuit (placed just before the flip-flop) adjusts the switching threshold of its inverter based on the output of the flip-flop in the previous cycle to reduce the charging/discharging time of the flip-flop's input capacitance. Moreover, the smaller input capacitance of the feedback equalizer reduces the switching time of the last gate in the combinational logic block. Overall, this reduces the total delay

of the sequential logic, which makes it more robust to timing errors and allows aggressive clocking to reduce the dominant leakage energy. In addition to reducing energy consumption, we also demonstrate how the tuning capability of the equalizer can be used to enable extra charging/discharging paths for the flip-flop input capacitance after fabrication to mitigate timing errors resulting from worse than expected process variations in the subthreshold digital logic. In general, our approach of using feedback equalizer to lower energy consumption and improve robustness is independent of the methodology used for designing a combinational logic block operating in the subthreshold regime. The main contributions of this paper are as follows.

1) We propose using an adaptive feedback equalizer circuit in the design of tunable subthreshold digital logic circuits. This adaptive feedback equalizer circuit can reduce energy consumption and improve the performance of the subthreshold digital logic circuits.
2) We present detailed analytical models (AMs) for performance and energy of the adaptive feedback equalizer circuit. These models can be easily used in combination with the existing performance and energy model for subthreshold circuits to generate subthreshold designs that meet energy and/or performance constrains.

II. RELATED WORK

Several techniques have been proposed to design robust ultralow power subthreshold circuits. As described earlier, transistor upsizing [2] and increasing the logic path depth [4], [5] can be used to overcome process variations. The use of gates of different drive strengths have also been proposed to overcome process variations [6]. A detailed analysis of the timing variability and the metastability of the flip-flops designed in the subthreshold region has been presented in [7] and [8], respectively. Lotze and Manoli [9] have used the Schmitt trigger structures in subthreshold logic circuits to improve the I_{ON} / I_{OFF} ratio and effectively reduce the leakage from the gate output node. Pu *et al.* [10] proposed a design technique that uses a configurable V_T balancer to mitigate the V_T mismatch of transistors operating in subthreshold regime. Zhou *et al.* [11] propose to boost the drain current of the transistors using minimum-sized devices with fingers to mitigate the inverse narrow width effect in the subthreshold domain. An analytical framework for subthreshold logic gate sizing based on statistical variations has been proposed in [12], which provides narrower delay distributions compared with the state-of-the-art approaches. Body-biasing has also been proposed to mitigate the impact of variations [13]. A controller that uses a sensor to first quantify the effect of process variations on subthreshold circuits and then generates an appropriate supply voltage to overcome that effect has been proposed in [14]. De Vita and Iannaccone [15] have used a current reference circuit to design a voltage regulator providing a supply voltage that makes the propagation delay of the subthreshold digital circuits almost insensitive to temperature and process variations. Using a differential dynamic logic in standby mode, Liu and Rabaey [16] propose to suppress leakage in the subthreshold circuits.

Error detection and correction techniques have been widely used to design resilient, energy-efficient above-threshold architectures [17]–[20]. Tschanz *et al.* [17] and Bowman and Tschanz [18] have used a tunable replica circuit (with 3.5% leakage power overhead, 2.2% area overhead), and error-detection sequential (with 5.1% leakage power overhead and 3.8% area overhead) to monitor critical path delays and mitigate dynamic variation guard bands for maximum throughput in the above-threshold regime. Using an adaptive clock controller based on error statistics, the proposed processor architecture operates at maximum efficiency across a range of dynamic variations. Bull *et al.* [19] applied Razor error correction technique (with 9.4% power overhead and 6.9% area overhead) to a 32-bit ARM processor with a micro-architecture design for energy-efficient operation through the elimination of timing margins. Whatmough *et al.* [20] applied Razor (with 16.9% power overhead and 1.59% area overhead) to a 16-tap finite-impulse-response (FIR) filter realizing a 37% improvement in energy efficiency. These error correction techniques could be potentially used in combination with our feedback equalization technique to improve robustness in sequential logic blocks operating in the subthreshold regime. We propose a circuit-level scheme that equalization technique in the critical path to mitigate the timing errors rising from aggressive voltage scaling and process variations in subthreshold digital logic circuits. It should be noted that we are not designing subthreshold communication circuits. We are proposing the design of subthreshold logic circuits that leverage principles of communication theory. Several authors have already used feedback-based techniques to boost the to improve the speed and power of on-chip global interconnects leading to 14% delay improvement over the weak low-voltage signals in global interconnections [21],[25]. Seo *et al.* [21] proposed the self-timed regenerator technique conventional repeater design in the above-threshold regime. Schinkel *et al.* [22] presented a pulse width pre-emphasis equalization approach with lower latency compared with the classic repeater insertion technique. Kim and Seok [23] proposed a reconfigurable interconnect design technique based on regenerators for ultra

Novelty Journals

ISSN 2394-9678

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dynamic-voltage-scaling systems to improve performance and energy efficiency across a large range of above-threshold supply voltages. Seo *et al.* [24] proposed the design of an adaptively controlled preemphasis transceiver to reduce intersymbol interference in on-chip signaling. Kim and Stojanovic [25] presented an energy-efficient transceiver design that performs feedforward equalization for repeaterless, high-performance on-chip communication.

III. ADAPTIVE EQUALIZED FLIP-FLOP VERSUS CONVENTIONAL FLIP-FLOP:

In this section, we first explain the use of the adaptive feedback equalizer circuit in the design of an adaptive equalized flip-flop (E-flip-flop) and then provide a detailed comparison of the E-flip-flop with the conventional flip-flop in terms of area, setup time, and performance. We propose the use of a variable threshold inverter [26] (Fig. 1) as an adaptive feedback equalizer along with the classic master-slave positive-edge-triggered flip-flop [29] (Fig. 2) to design an adaptive E-flip-flop. This adaptive feedback equalizer circuit consists of two feedforward transistors (M1 and M2 in Fig. 1) and four control transistors (M3 and M4 for feedback path 1

Table I: Propagation Delay

Minimum supply Voltage (mV)	Delay NE-logic (ns)	Delay E-logic (ns)	Delay Buffer NE-logic (ns)
950	681.5	881.00	681.2
900	681.2	880.80	681.1
850	681.0	880.40	680.5
800	680.4	880.00	680.0
750	680.0	879.00	679.0
650	678.0	8.77	679.0
620	677.0	876.00	675.0
550	672.0	872.00	665.0

Table II: Leakage Power

Minimum supply Voltage (mV)	Leakage Power E-logic(µW)	Leakage Power NE-logic (µW)	Leakage Power Buffer NE(µW)
950	6.1	6.6	4.8
900	4.9	6.0	4.3
850	4.5	4.2	4.9
800	3.7	4.0	4.9
750	3.3	3.7	4.7
650	2.6	3.0	4.5
620	2.4	2.8	4.2
550	2.2	2.0	2.9

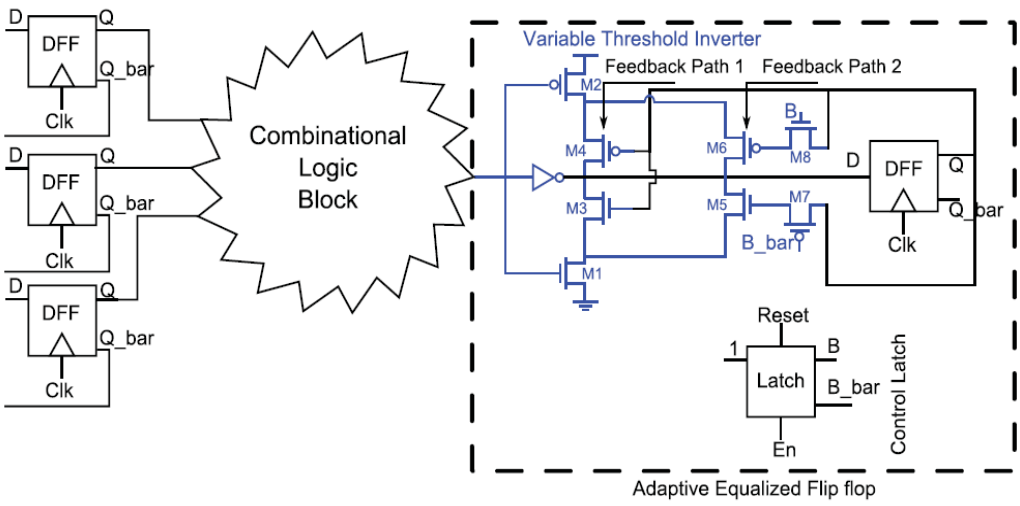

Fig 1: Adaptive feedback equalizer circuit with multiple feedback paths (designed using a variable threshold inverter) can be combined with a traditional master-slave flip-flop to design an adaptive E-flip-flop.

Novelty Journals

ISSN 2394-9678

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that is always ON and M5 and M6 for feedback path 2 that can be conditionally switched ON post fabrication in Fig. 1) that provide extra pull-up/pull-down paths in addition to the pull-up/pull-down path in the static inverter for the Data Flip-Flop input capacitance. The extra pull-up/pull-down paths are enabled whenever the output of the critical path in the combinational logic changes. The control transistors M5 and M6 are enabled/disabled through transistor switches (M7 and M8) that are controlled by an asynchronous control latch. The value of the static control latch is initially reset to 0 during chip bootup. After bootup, if required a square pulse is sent to the En terminal to set the output of the latch to 1 to switch ON M7 and M8, which enables feedback path 2.

The adaptive E-flip-flop effectively modifies the switching threshold of the static inverter in the feedback equalizer based on the output of the flip-flop in the previous cycle. If the previous output of the flip-flop is a 0, the switching threshold of the static inverter is lowered, which speeds up the transition of the flip-flop input from 0 to 1. Similarly, if the previous output is 1, the switching threshold is increased, which speeds up the transition to 0. Effectively, the circuit adjusts the switching threshold and facilitates faster high-to-low and low-to-high transitions of the flip-flop input. Moreover, the smaller input capacitance of the feedback equalizer reduces the switching

time of the last gate in the combinational logic block. Overall, this reduces the total delay of the sequential logic. The simulation result of the adaptive feedback equalizer circuit with two different feedback paths in the subthreshold regime is shown in Fig. 3.

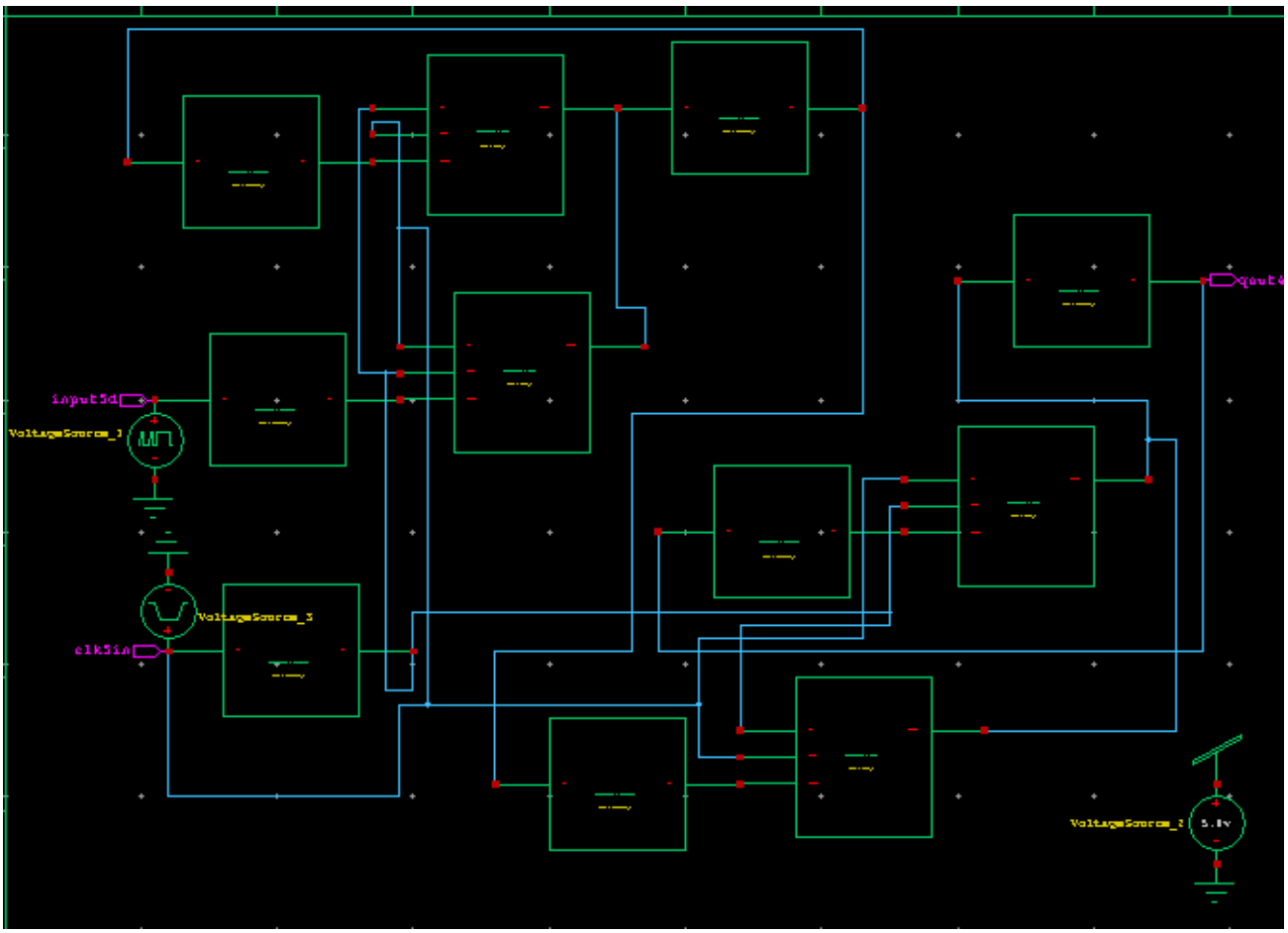

Fig 2: Circuit diagram of classic master-slave positive edge- triggered flip-flop

The adaptive E-flip-flop has eight more transistors than the conventional master-slave flip-flop [29]. Compared with a classic master-slave flip-flop with 22 transistors [seven inverters and four transmission gates (TGs)], the area overhead of the adaptive E-flip-flop is 36%. The area has overhead of the control latch with ten transistors (three inverters and two TGs) 45%. This area overhead gets amortized across the entire sequential logic block.

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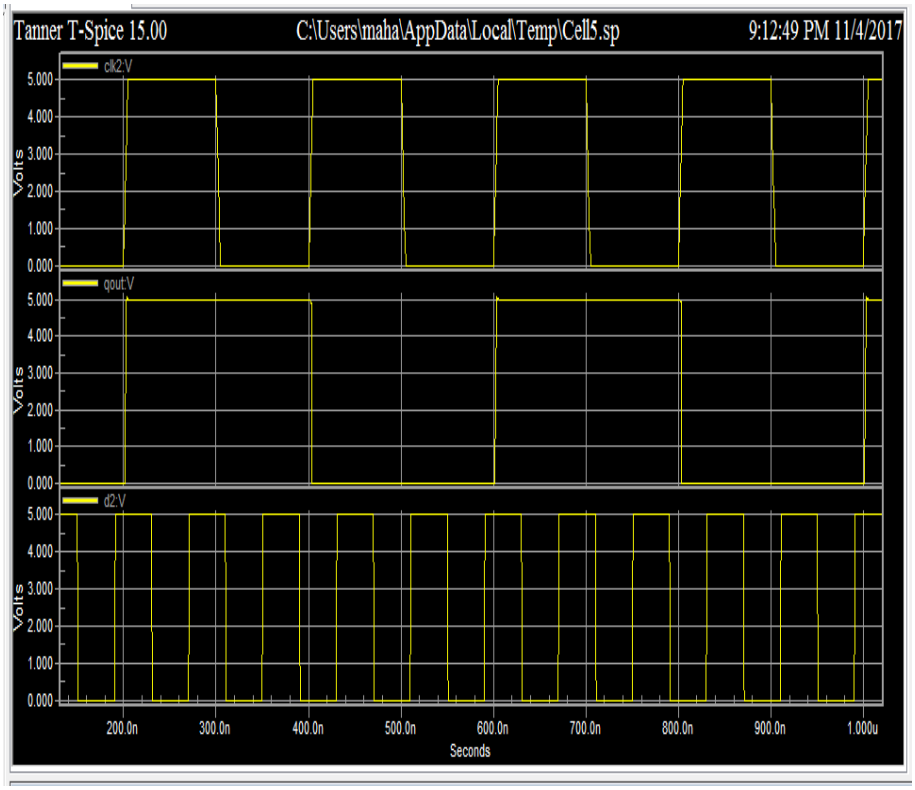

Fig 3: Simulation result of classic master-slave design, positive-edge-triggered flip-flop

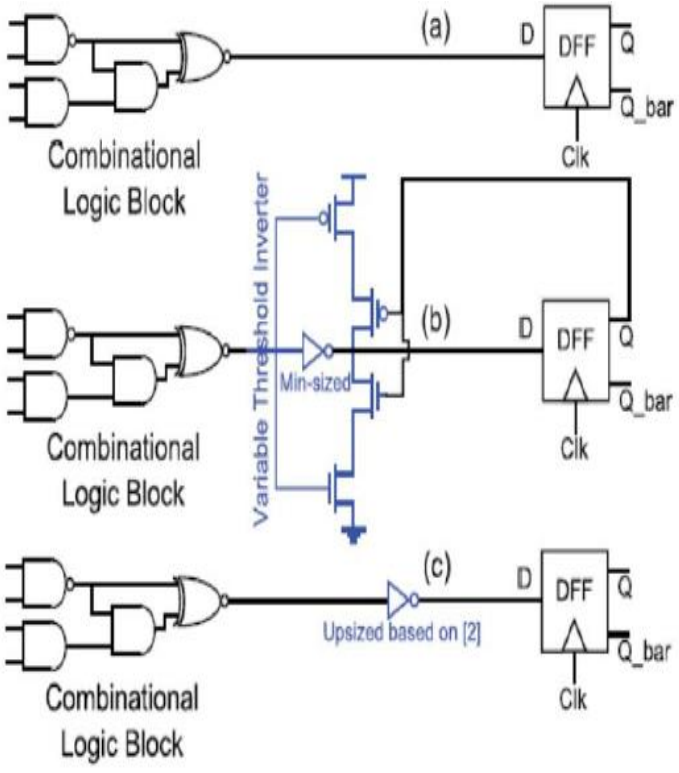

Fig 4: Block diagram of (a) original nonequalized (b) equalized design with one feedback path ON, and (c) Buffer- inserted nonequalized design.

IV. POWER ANALYSIS

The leakage power, propagation delay and the product of power and delay are shown in (table I, II, III) when the input voltage is reduced. The propagation delay of the Nonequalized flip-flop is reduced from 681.5μs to 672μs. The proposed low power subthreshold a logic circuit is used for adaptive feedback equalizer circuit is designed.

TABLE III: POWER DELAY PRODUCT

Min. supply voltage (mV)	PDP NE-logic (nW)	PDP E-logic (nW)	PDP buffer NE-logic (nW)
950	4157.2	5814.6	3269.7
900	3338.0	5284.4	2928.7
850	3064.5	3697.6	3332.6
800	2516.4	3520.0	3334.4
750	2244.0	3252.3	3191.3
650	1762.8	2631.0	3055.5
620	1624.8	2452.8	2835.0
550	1478.4	1744.2	1928.5

V. CONCLUSION

The proposed adaptive feedback equalizer circuit is used to reduce the normalized variation of propagation delay along the critical path and the dominant leakage power of the digital CMOS logic operating in the subthreshold regime. Adjusting the circuit switching threshold of the gates before the flip-flop based on the gate output in the previous cycle, the adaptive feedback equalizer circuit enables a faster switching of the gate outputs and provides the opportunity to reduce the leakage power of digital logic in weak inversion region. The adaptive feedback equalization circuit to the propagation delay of Nonequalized flip-flop from 681.ns to 672ns, the power consumption of Equalized flip-flop from 6.6μW to 2.0μW and Power Delay product reduced in different input voltage.

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